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12GHz divide by 1000 prescaler

Expanding a frequency counter by adding an external precaler is a simple and inexpensive option if you wish to measure higher frequencies. This new divider module includes the 10GHz band and cuts out some tedious conversion by having a decimal division factor of 1000.

1. Introduction

A high quality, universal 5GHz frequency divider has already been presented in [1].
However, the requirements set for the divider module described below were rather different:
It was to cover the 10GHz band and was to have a decimal divider factor. The high division factor of 1000 means the module can be connected to almost any frequency counter. It is also a simple way of processing the divided signal (TTL level) for special tasks, using a micro controller. Thus, for example, a simple 12MHz frequency counter circuit could be created and combined with the divider module to display and monitor the output frequency of a transmitter.

2. Resolution and accuracy

Determining the frequency of a signal source is a fundamental measurement in high frequency measuring techniques, and it must, above all, be carried out very accurately. In this context, carrying out a measurement is nothing but a comparison between a known and an unknown value. The more accurately the known comparison value can be represented, the more accurate the measurement will be.

In frequency measurement, the frequency, *f*, is the reciprocal value of the period, *t*, which is a temporal value. Yet time itself is one of the most accurately reproducible experimental values. Thus frequency measurement becomes one of the most accurately performed measurements.

To measure a frequency, we need a counter, which counts the number of cycles in a specific period of time (gate time) and then standardises on a gate time of one second. The counter is usually a digital circuit, e.g. a micro controller, which is started and stopped by a quartz crystal timed gate.

The uncertainty, δf, of the frequency measurement is made up of the accuracy of the reference frequency of the time base, δf_{TB}, and the uncertainty of count-

ing. The uncertainty of counting amounts to ±1 cycle, since the gate time is not synchronised with the signal frequency to be measured. Thus, depending on the position of the oscillations, one counting pulse more or less can be generated during the gate time. Depending on the length of the gate time and the level of the counting frequency, this error appears more or less pronounced. [2]

$$\delta f = \frac{\Delta f}{f} = \frac{f \cdot \delta f_{TB}}{f} + \frac{\frac{1}{t_{Tor}} \cdot divisionfactor}{f} = \delta f_{TB} + \frac{divisionfactor}{f \cdot t_{Tor}}$$

Time base + uncertainty of counting

where:

δf = relative uncertainty of frequency measurement,

Δf = absolute uncertainty of frequency measurement,

δfTB = relative uncertainty of reference frequency (time base),

tTor = time gate,

f = frequency to be measured

In high frequency measurement (>100MHz), a frequency divider must first be used to split these frequencies into smaller frequencies which the counter circuit can process. This does not influence the part of the total error originating from the reference frequency. It is only the influence of the counting uncertainty (usually small) which increases.

The resolution of a frequency counter is just as important as the uncertainty. This is reciprocal to the gate time, which can be made clearer by an example:

A frequency counter has to count a frequency of 10MHz. If it counts the number of cycles in a gate time of 1 second, it will count 10 million. It has thus counted with a resolution of 10^6 Hz / 10^6 oscillations = 1Hz.

If it counted with a gate time of 100ms, it could count only a million cycles in this time. The resolution would thus be 10^6 Hz / 10^5 oscillations, i.e. 10Hz.

It should be pointed out that frequency counters with reciprocal counting methods attain a higher resolution (usually by a factor of 10 or 100) for the same gate time, due to their special mode of functioning.

The resolution of a frequency counter with a prescaler connected in series deteriorates by the value of the division factor. This is because the actual counter can only count the lower frequency that is produced by the divider as an input signal.

$$\mathrm{Re}\,solution = \frac{1}{T_{Tor}} \cdot didvsionfactor$$

Thus the division factor for a prescaler should be selected as low as possible. This will give the highest resolution for a given gate time!

The division factor of 1000 selected here must now be analysed more closely:

Advantages:

- Conversion on the frequency counter can be carried out very simply. For example, a display of 10MHz corresponds to an input frequency of 10GHz.
- The existing frequency counter needs a frequency range of only 12MHz to be able to make full use of the frequency divider.
- Simple further processing for micro computer circuits based on the low output frequency with TTL level.

Disadvantages:

- The resolution is reduced by a factor of 1000. So, for a measurement time of one second, we obtain a resolution of 1kHz, and at 100ms gate time only 10kHz.
- This disadvantage, though, must be examined still more closely with

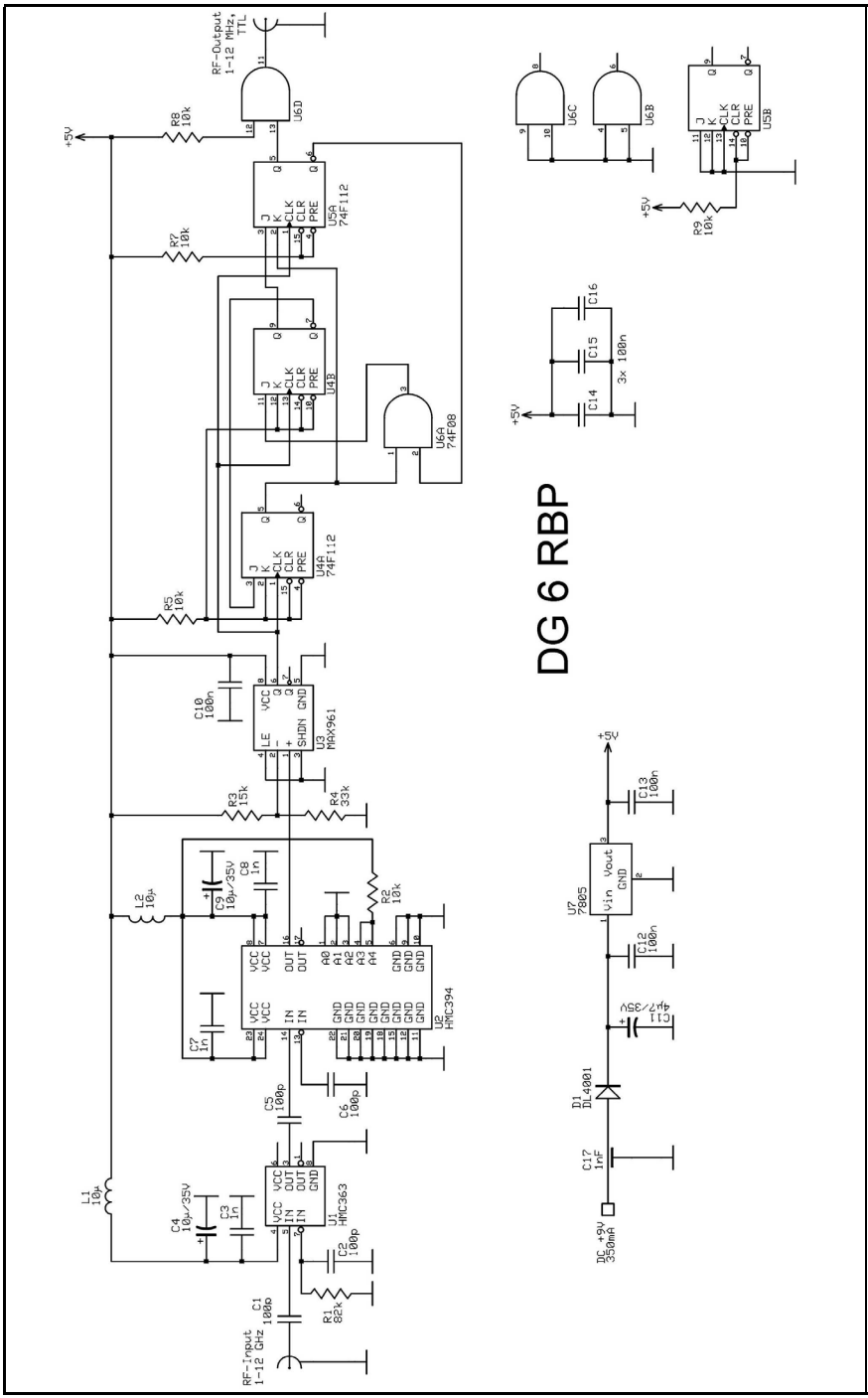

Fig 1: Circuit diagram for 12GHz divide by 1000 prescaler

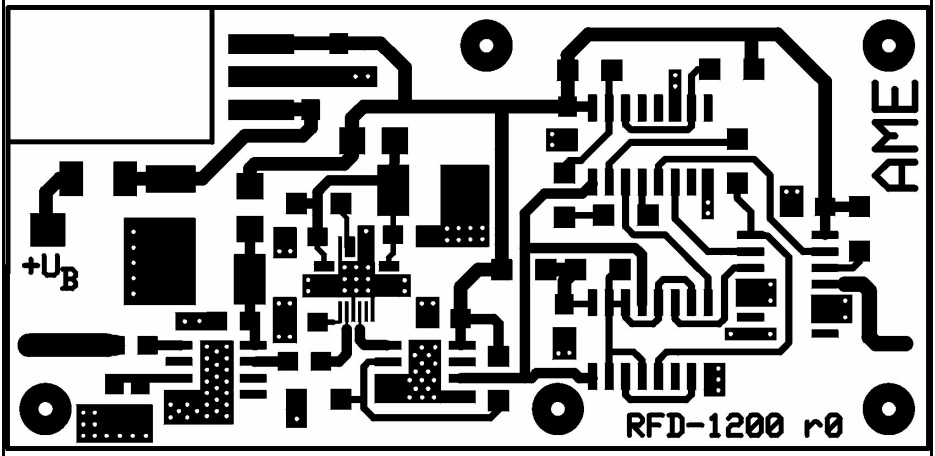

Fig 2: Printed circuit board layout for 12GHz divide by 1000 prescaler.

regard to the combination of a frequency counter and a prescaler! There are two important points to be taken into account here:

1) Practically all frequency counters in the medium price range can count directly only up to about 100MHz. All higher frequencies (e.g. 1.3GHz input) are divided down first, frequently by a factor of 64.

2) Does the uncertainty of the time base allow for meaningful measurements at high resolution?

Re. point 1:
The present 12GHz frequency divider divides a frequency from 12GHz to 12MHz. A typical frequency counter can count these frequencies directly, with a resolution of 1000Hz at a gate time of 1 second.

If the 12GHz frequency divider divided by only 10, we would have a frequency of 1.2GHz. A typical frequency counter would internally divide this again by 64 before it could count it. The resolution would then be 640Hz for a gate time of 1 second. So we would gain nothing.

Re. point 2:
A normal frequency counter in the medium price range has a quartz crystal as reference, with a typical relative uncertainty of 10^{-6}. If we were to measure a frequency of 10GHz (10^{10}Hz) by direct counting, i.e. without a frequency divider or with a divider factor of 1, with a gate time of 1 second. At the end of the day the measurement would have an absolute uncertainty of $10^{10}*10^{-6} = 10^{4}$Hz due to the reference frequency, plus 1Hz due to the counting uncertainty, which thus gives us 10.001kHz.

If we use the frequency divider, we obtain a resolution of 1kHz for the same input frequency and the same gate time. At the same time, we obtain an absolute uncertainty of 10kHz due to the reference frequency, plus 1kHz counting uncertainty. This gives a total error of 11kHz. As can be seen, the error in both cases, i.e. direct counting or with a frequency divider connected in series, exceeds the resolution with a divider. So it does not make sense to use the divider factor to increase the resolution.

Thus the division factor of 1000 is no disadvantage for an average frequency counter in the medium price range!

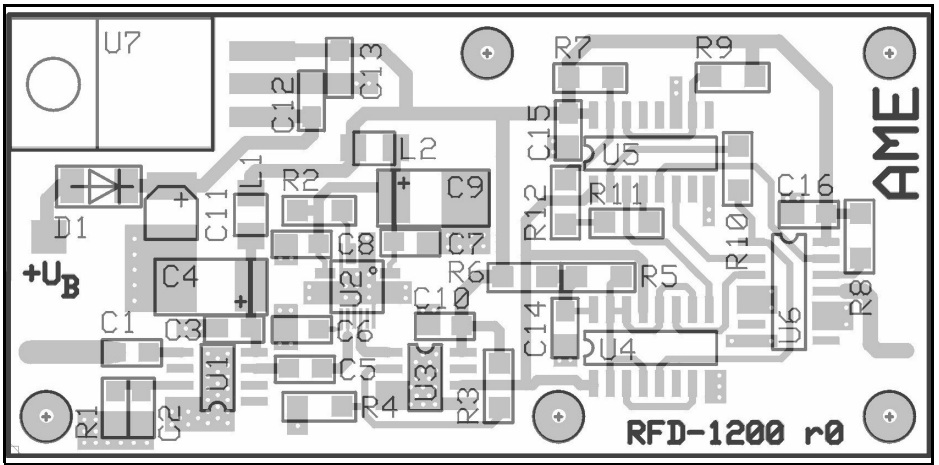

Fig 3: Component layout for 12GHz divide by 1000 prescaler.

Only very high quality equipment fitted with a precision ovened quartz crystal attains a relative reference frequency uncertainty in the region of 10^{-9} to 10^{-11}. The resolution could be meaningfully increased here with a smaller divider factor, but only if the counter can also count the input frequency divided by the divider directly (i.e. without an additional internal prescaler)!

3. Circuit description

Fig. 1 shows the circuit diagram of the frequency divider. The input signal passes through the coupling capacitor, C1, to an HMC-363 12GHz divider (U1).

Unfortunately divider modules oscillate when there is no input signal, and this one is no exception. This behaviour is a problem when expanding a frequency counter. Without an input signal, the equipment registers an unstable frequency that is not really present. With many modules this can be prevented if the inverting input is earthed through a resistance in the kΩ range. The module usually reacts to a reduction in resistance with a reduction in the tendency to oscillate, but it then also has reduced sensitivity. In the present case, the tendency to oscillate could be suppressed using the resistance R1, without having too much of a detrimental effect on the sensitivity.

The signal, divided by 8, then comes to the 5 bit counter, U2 (HMC-394), which is programmed with the connections A0-A4 for a division factor of 25. Here is a useful tip for anyone who is feeling a little irritated looking at the wiring diagram: according to the data sheet [3], you should select precisely the desired divider factor less 1.

The output signal from U2 is a type of square wave signal with a DC offset. In order to obtain a TTL signal from it, which is what the subsequent TTL divider needs, we use the U3 (MAX 961) rapid comparator from Maxim. It compares the signal from U2 with the threshold voltage from the resistance divider, R3 / R4, and thus generates a clean square wave signal at the output with an amplitude of 0V or 5Volts.

In the end, it has proved necessary to develop another synchronous counter

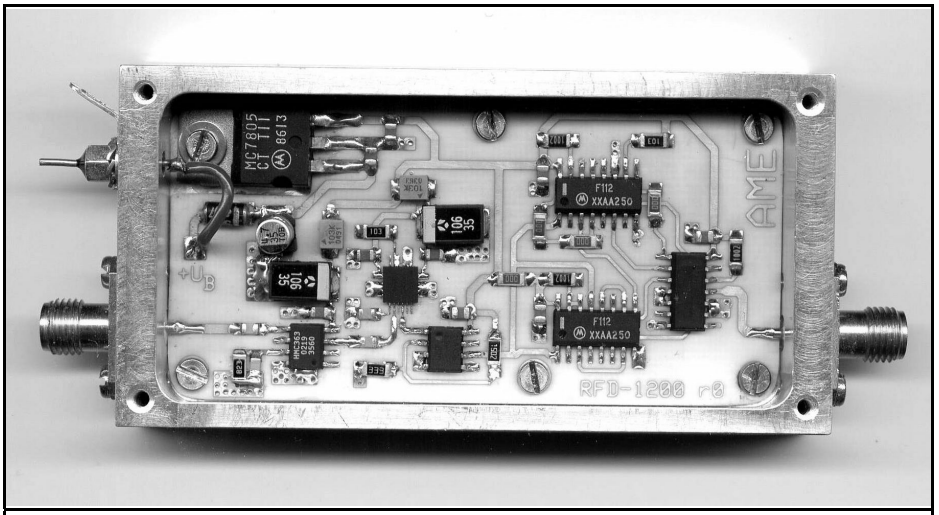

Fig 4: Completed prototype of the 12GHz divide by 1000 prescaler.

manually as a TTL divider by five. To be able to display the numbers 0 to 4, we need 3 Bits, and thus we also need the three JK flip-flops, U4/U5 (each 74F112).

The signal from the TTL divider is fed to the output via the free AND gate used as a buffer.

The operating voltage of the divider module (approximately 9 to 15V) is fed through the feedthrough capacitor, C17, and the reverse battery protection diode D1 to the voltage regulator, U7. This generates a regulated voltage of 5V for the divider modules. The supply voltages for U1 and U2 are fed through LC filters to reduce any RF residue.

4. Assembly of circuit

The circuit diagram was used to develop a board layout (Fig. 2) with the dimensions 71mm x 34mm This size was selected because there were suitable tinplate housings available. However, these are advantageous only if the price plays a significant role. A milled aluminium housings is definitely preferable. If a tinplate housing is used, a suitable heat sink should be provided to cool the voltage regulator and the divider module (especially U2). The prototype of the frequency divider was incorporated into a milled aluminium housing.

The base material used for the through hole plated board was 0.81mm thick RO4003C substrate from Rogers. This board material has outstanding high frequency characteristics, but it can be worked like standard epoxy (FR4) and can be obtained at budget prices.

The 50 Ohm track width is about 1.8mm. This width should be maintained, at least from the RF input to the first divider IC, U1. This track width can not always be adhered to as the RF signal moves over the board, since the connections to the divider ICs must be made very narrow. However, this is no great tragedy, provided the tracks remain very short.

The components are mounted by hand in accordance with the component drawing (Fig. 3). Problems arise only with the divider, U1, and the 5 bit counter, U2.

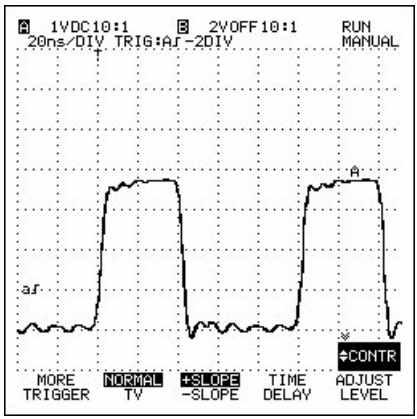

Fig 5: Output signal for 10GHz input.

The IC, U1, must be soldered to the earth area on its underside (!)! This can be done through prior tin plating, or better using solder paste and hot air (or a hot plane). Things become more difficult with U2, the connections of which are, to a very large extent, on the underside of the chip, and where the pin distance, 0.5mm (!), is extremely small.

Anyone venturing to copy the divider should therefore have a lot of experience in soldering small SMD components.

By the way, the divider, U2, runs relatively warm, its current consumption being just on 200mA. It is cooled via its earth area and the through plating to the aluminium housing base.

Fig. 4 shows the prototype of the divider module.

5. Parts list

SMD capacitors:		
C1,C2,C5,C6	100pF	0805
C3,C7,C8	1nF	0805
C10,C12-C16	100nF	0805
C4,C9	10µF / 35V	SMD tantilum
C11	4.7µF / 3V	SMD electrolytic capacitor
C17		1nF feedthrough capacitor, Actipass FC-102P-10A
L1,L2		10µH SIMID 1210
R6,R10-R12		0Ω, 1206
R2,R5,R7-R9		10kΩ, 1206
R3		15kΩ, 1206
R4		33kΩ, 1206
R1		82kΩ, 1206
D1		DL4001
U1		HMC 363 S8G
U2		HMC 394 LP4
U3		MAX961CS8
U4, U5		74F112 SMD
U6		74F08, SMD
U7		7805
1 x		LP DG6RBP-006
1 x		Aluminium milled housing
or		
1 x		Tinplate housing 71 x 34 x 30mm
2 x		SMA sockets with 4 hole flange

6. Measurement results

To test the frequency divider, a signal with a power of 1mW (0dBm) was fed in from a 20GHz HP 83732A signal generator, and the frequency was varied between 500MHz and 15GHz. The behaviour of the divider was monitored using frequency counters and an oscilloscope. No functional errors could be observed here. The output signal is shown in Fig. 5 for an input frequency of 10GHz.

If the divider is operated without an input signal, the output is either low or high level, depending on the counting step of the TTL divider. A tendency to oscillate without an input signal arose only where relatively long coaxial lines were connected without load.

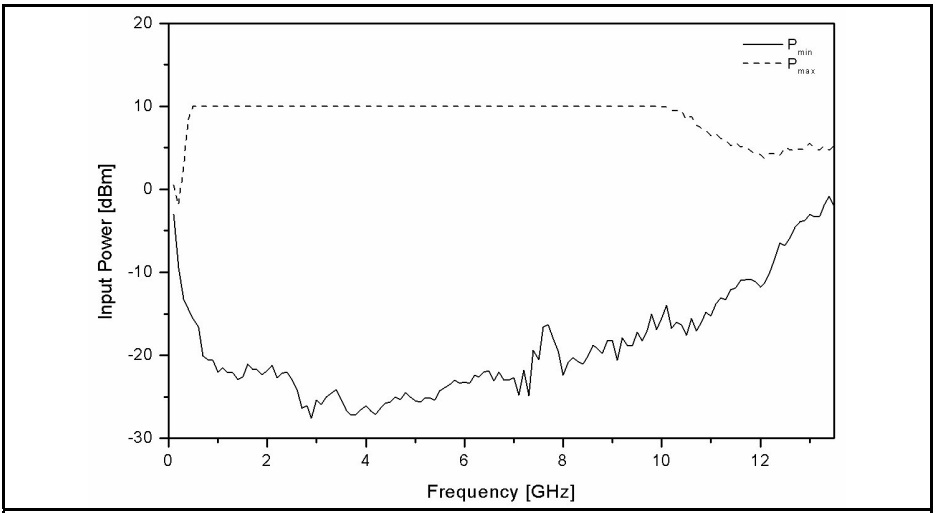

Fig 6: Minimum input power requirement for the 12GHz divide by 1000 prescaler.

In a second test, the power was varied at constant frequency (1GHz). In this test, it was established that at very low power levels false division factors arise! The precise input power level at which this behaviour begins depends on the input frequency and establishes the minimum level required for the frequency divider.

This minimum input power requirement for the divider module is shown in Fig. 6.

7. Technical data

- Frequency range
  - Input min. 0.5 to 12GHz
  - Output 0.5 to 12MHz
- Divider factor 1000
- Input level approx. 10 to +5dBm
- Output level[1] 5V TTL
- SWR (HF input) typ. 2...6
- Tendency to oscillate with an open input - no[2]
- Connectors SMA sockets
- Operating voltage +15VDC
- Current consumption max. 350mA

[1] Without an input signal, there is either a low or a high level at the output.

[2] When relatively long, open coaxial cables are connected, or in similar situations, in certain circumstances a tendency to oscillate can arise when there is no input signal.

8. Literature references

[1] Alexander Meier: Pre divider (:10) to 5GHz, VHF Communications 1/2002, pp 22 - 26

[2] Thumm/Wiesbeck/Kern: High-frequency measuring technique, Teubner Verlag 1997, Stuttgart

[3] Data sheet HMC-394, Hittite Microwave Corporation, 12 Elizabeth Drive, Chelmsford MA 01824