Konrad Hupfer, DJ1EE

400W power amplifier for 2m

Because the 2m band is enjoying an increase in popularity a power amplifier with the maximum output of 400 - 450W with a supply voltage of 28 – 32V is described in this article. The active device was chosen as a proven "VHF workhorse" from the manufacturer SEMELAB. It is very robust; the load VSWR may vary up to 20:1 thus giving more scope for output network optimisation without destroying the semiconductor. Full data for the transistor can be found in the datasheet [1]. The circuit is not complicated yet has good characteristics.

1. The circuit

The critical part of a transistor power amplifier circuit (Fig 1) is the output network. A mismatch at the output represents a danger to the semiconductor. Therefore the matching circuits shown in Fig. 2 will be described in more detail in this article.

A narrow band solution would be sufficient for the 144MHz to 146MHz frequency range, it is nevertheless advisable to use a wider band solution in order to allow for adjustment tolerances and alignment sensitivity. The input and output matching circuits NW1 and NW4 consists of λ/4 matching transformers (25Ω coax cable), they also provide a 50Ω asymmetric to 12.5Ω symmetric transformation. The networks NW2 and NW3 are very simple L/C circuits with inductances made from individual striplines.

1.1. Design of the circuit for network NW3

The λ/4 matching transformer NW4 is made from 25Ω coaxial cable (flexible or Semirigid cable should be used with an outside diameter not less than 3mm because of the 400W output power that it must handle) that transforms the asymmetric 50Ω load R_L to 2 x R'_L = 2 x 6.25Ω = 12.5Ω.

To make the computation a bit clearer, Fig 3 shows that the real load is divided from 12.5Ω to 2 x 6.25Ω. The network NW3 must be designed to match the optimal load resistance R'_{opt} at half of the total output of 200W with the internal values of the transistor shown in Fig 4. The value R'_{opt} is shown in the SEMELAB data sheet. The internal load resistance R'_{DS} can be determined from the effective RF Drain voltage V'_{RF} at 200W. The effective RF voltage is close to the supply less "the bottoming voltage" V_K (assumed to be 3V):

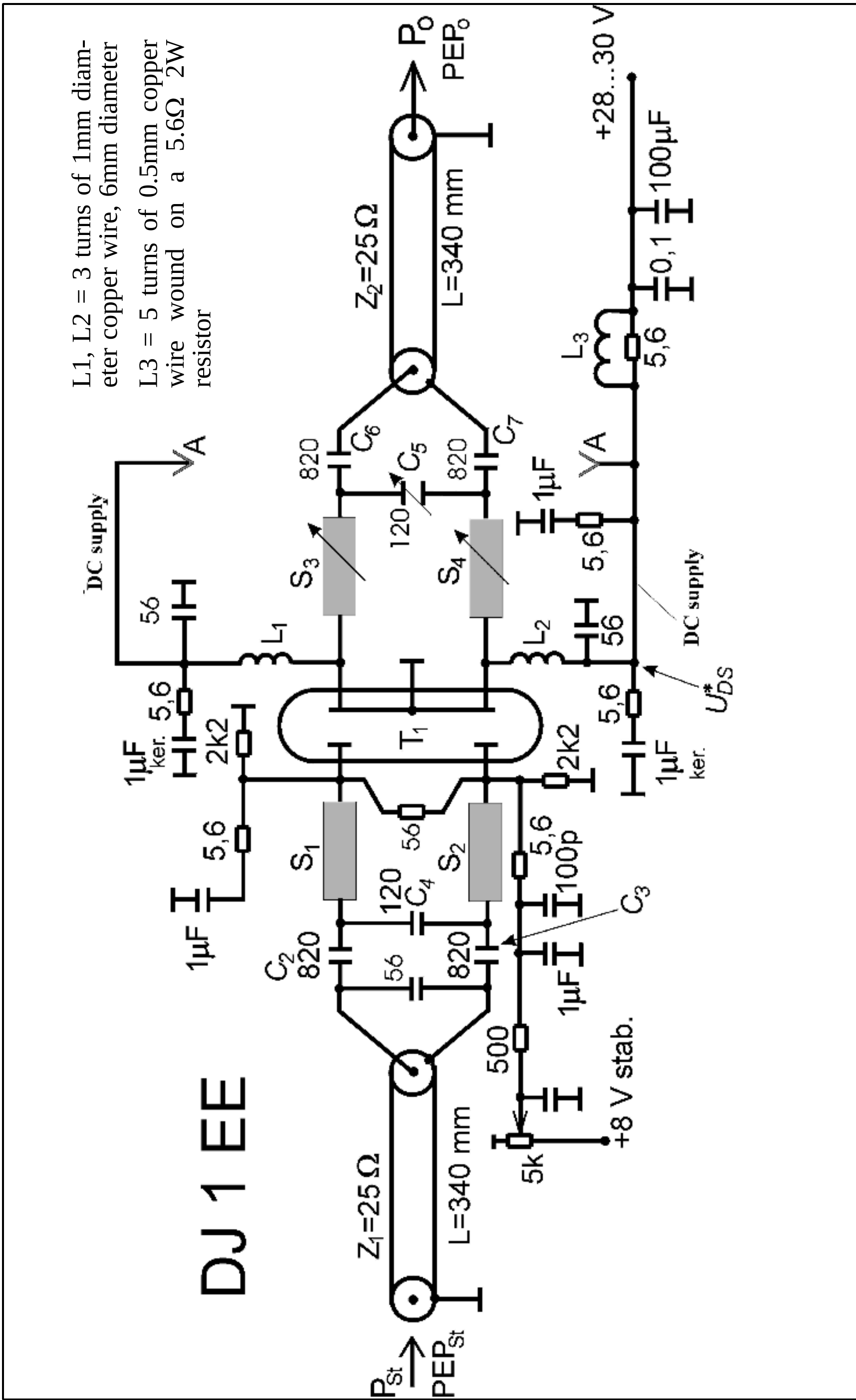

Fig 1: Circuit of the 400W 2m power amplifier.

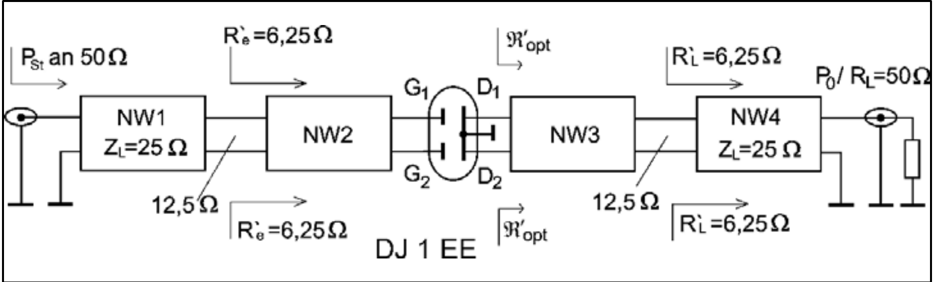

Fig 2: Block diagram of the 400W 2m power amplifier.

$$R'_{DS} = \frac{(U - U_K)^2}{2 \cdot P_o} = \frac{(28-3)^2}{400} = 1.56\Omega$$

In parallel with this is an output capacitance C_{ob} = 190pF (see data sheet). The effective capacity is:

$$C'_{ob} = 1.3 \cdot C_{ob} = 1.3 \cdot 190 = 250\,pF$$

The inductance of the drain connection is taken from the SEMELAB data and is 0.63nH.

1.1.1. Calculating the value of L1 (Fig 4)

L1 is made from a small low impedance stripline. The transformation procedure can be seen using a Smith chart. The Smith chart program by Fritz Dellsperger [2] was used for this process and found to be extraordinarily helpful for this task. The Smith chart in Fig 5 is standardised for the terminal resistance R'_2 = 6.25Ω, the internal load resistance R'_{DS} = 1.56Ω and the goal value R'_L = 6.25Ω can be seen. The chart is simplified to make it

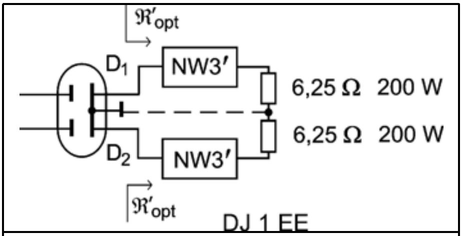

Fig 3: Network NW3.

easier to understand. Point 1 (Z_1) on the real axis represents R'_{DS} = 1.56Ω. C'_{ob} = 250pF is point 2 on the conductance circle. The bond inductance is a series inductor L = 0.63µH and is represented as Z_2 = 1.4 + j0.5Ω giving point 3. This is the impedance at the drain connector lug; Z_3 = 1.4 + j0.1Ω. This “transistor connection resistance” is now transformed with an inductance, formed by striplines, S3 and S4, on the circle around the centre of the diagram to point 4 giving Z_4 = 1.4 + j2.6Ω. This is the intersection with the conductance circle corresponding to the target resistance Z_5 = 6.25 +j0Ω.

The stripline width W was selected as 8mm and the substrate thickness, H, used was 0.83mm. The characteristic impedance Z_0 is given by:

$$\frac{W}{H} = \frac{8mm}{0.83mm} \quad \text{gives } 28.4\Omega$$

This is for a dielectric constant ε_R = 1. In reality the characteristic impedance of the striplines S3 and S4 are 16.5Ω because the substrate has a dielectric constant ε_R = 3.3. The inductance of this stripline is 2.8µH and is “quasi-stable” the length of the line is l = 30mm. The inductance of this very short line is independent of ε_R!

If a 320pF capacitor is connected from point 4 to ground then a real resistance of 6.25Ω is achieved (point 5 on the Smith chart). This matches one half of the

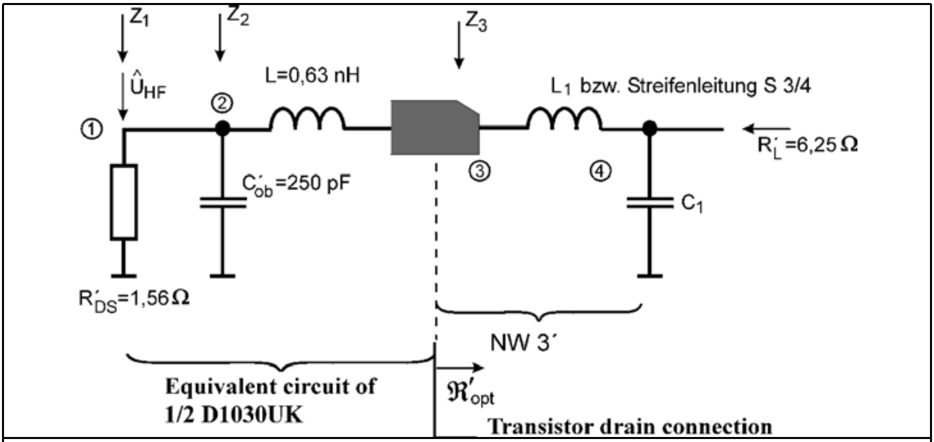

Fig 4: The equivalent circuit of 1/2 D1030UK.

power transistor to 6.25Ω. For the push-pull circuit twice this value is used, see Fig 6. Because the "virtual ground" does not exist, the two single capacitors in Fig 6 are combined into a single capacitor (2 x 320pF in series = 160pF).

If the output networks are used with the calculated values the output power will be approximately 250 to 300W. The transistor equivalent circuit used do not exactly correspond to the actual values partly because of differences in the mounting of the transistor. In order to achieve the maximum output power of 400W with good efficiency (~70%), changes in the striplines S3 and S4 as well as the capacitor C5 are required. This is shown in Fig 1 by the variable arrow on these components. This tuning was carried out while watching the efficiency and the values shown in Fig 7 were the result.

The characteristics of the output stage with a supply voltage V_{DS} of 28V and 32V are shown in Fig 8.

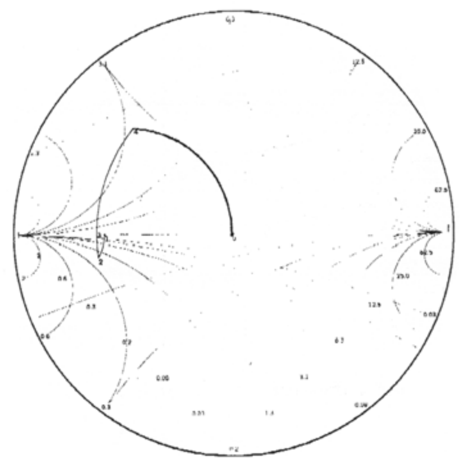

Fig 5: Smith chart showing the transformation to 6.25Ω.

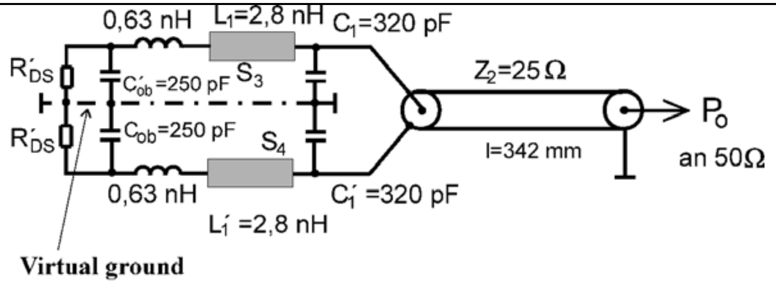

Fig 6: Circuit showing the two the two halves of the push-pull amplifier.

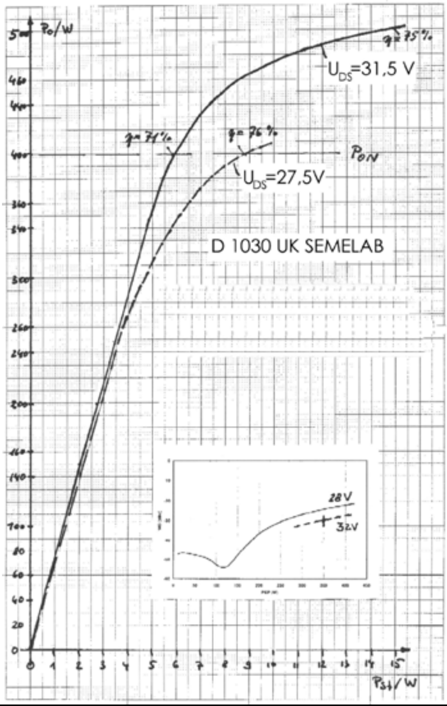

Fig 8: Output characteristics of the D1030UK.

1.2.1. Measured performance

The performance of the amplifier was measured with the equipment shown in Fig 13. The results for a supply voltage of 28V are shown in Table 1 and for a 32V supply voltage in Table 2.

1.3. Input matching

The input impedance of ½ D1030UK has the typical values shown in Fig 9.

R'_{GS} is found, like R'_{DS}, in the data sheet [1]. R'_{GS} can be transformed to 6.25 +j0Ω using a simple L/C circuit. The inductor is again made from a stripline. The transformation to 50Ω is achieved with λ/4 matching transformers made from 25Ω coax cable; thin cable is sufficient here because the power is low. Using the values calculated using a Smith chart, the input matching from 5:1 to 2:1 is achieved. The striplines and capacitors must be optimised as shown in Fig 10. Unlike the output the input can be trimmed to give a return of zero.

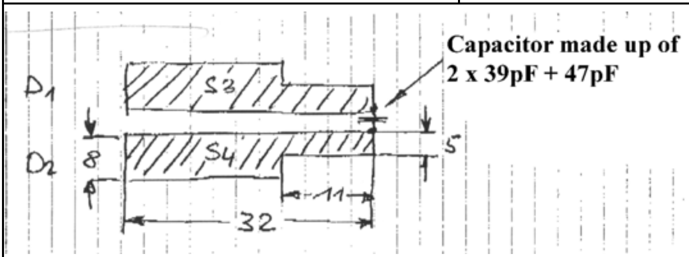

Fig 7: Dimensions of striplines S3 and S4 after optimisation.

Table 1: Measured parameters at 28V.

U_{DS} = 28V, I_D = 1.7A, f = 145MHz

CW:	P_o	400W
	P_{ST}	8.9W
	Efficiency	75%
	U'_{DS}	58V
Harmonics:	2 x f_0	-49dB
	3 x f_0	-44dB
SSB power:	PEP_0	300W
	PEP_{ST}	4.7W
	FMD_3	-29 to 31dB
	FMD_5	-35B
	Efficiency	49%

Table 2: Measured parameters at 32V.

U_{DS} = 32V, I_D ≈ 1.8A, f = 145MHz

Po/W	P_{ST}/W	I_D/A	G/dB	Effic%
50	0.7	6.8	18.7	24
100	1.35	9.2	18.9	
200	2.7	12.7	18.7	
300	4.3	15.9	18.5	
350	5.0	17.0	18.5	
400	5.9	18.1	18.3	71
450	8.2	19.6	17.4	74

SSB power	PEP_o	350W
	IM_3	-30dB

Maximum drain voltage:

(DC + RF) ≈ 65V for P_o = 480W

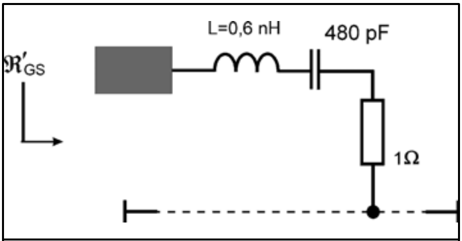

Fig 9: The input equivalent circuit.

2. Mechanical construction

Fig 12 shows the construction of the amplifier. The 50 x 150mm baseboard is fitted to the large 150 x 120 x 80mm heatsink as shown in Fig 11. The baseboard is 1.6mm thick copper clad FR4 material; the upper surface is the RF and DC ground. So that fitting the power transistor does not interrupt this ground, a very thin copper foil (~ 0.1mm) is fitted into the cutout for the transistor. The striplines are individually cut from 0.83mm thickness material and soldered to the baseboard ground surface. The DC wiring can take place as desired. Good heat transfer between the foil, transistor and heatsink is extremely important. Spread thermal compound on the indi-

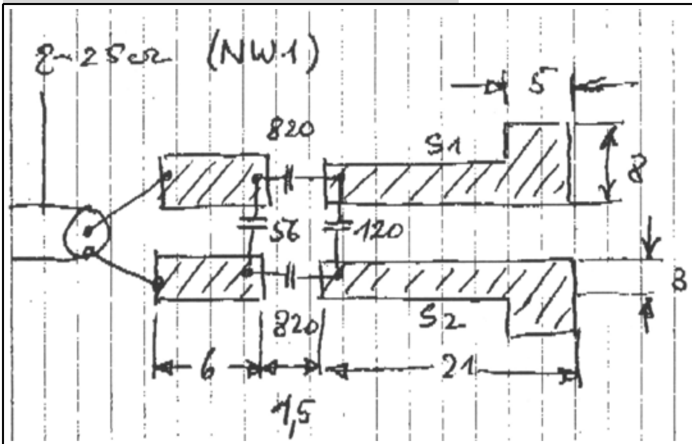

Fig 10: Dimensions of striplines S1 and S2 after optimisation.

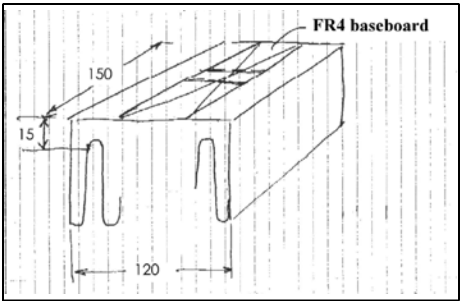

Fig 11: The heatsink and baseboard.

vidual surfaces very thinly because only the pores in the metal are to be filled! The heatsink should be well cooled with the aim of a maximum flange temperature of 60°C with a PEP output of 300W.

3. References

[1] SEMELAB, web: www.semelab.co.uk. The data sheet for the D1030UK can be downloaded from http://www.semelab.co.uk/pdf/rf/D1030UK.pdf

[2] Fritz Dellsperger, Smith chart program and Smith chart tutorials, email: fritz.dellsperger@isb.ch, web: http://www.fritz.dellsperger.net/

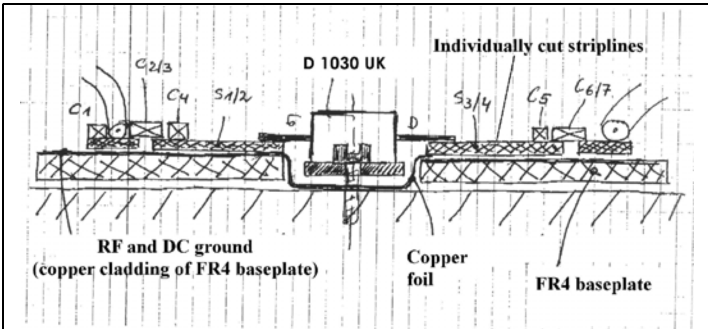

Fig 12: The mechanical construction of the 400W 2m power amplifier.

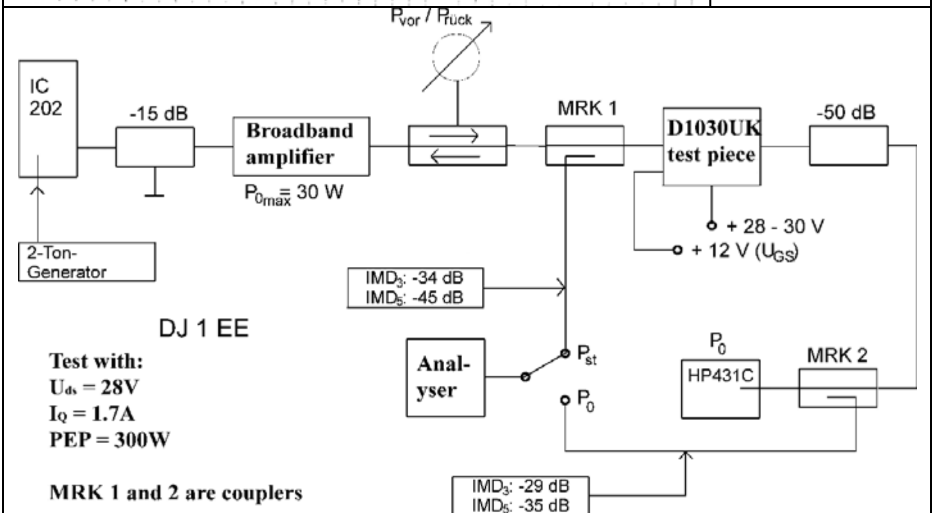

Fig 13: Block diagram of the performance measuring equipment.